Comprehensive Approach to MuGFET Metrology

[1]G.F. Lorusso, [1]P. Leray, [1]T. Vandeweyer, [1]M.Ercken, [1]C. Delvaux, [1]I. Pollentier, [1]S. Cheng, [1]N. Collaert, [1]R. Rooyackers, [1]B. Degroote, [1]M. Jurczak, [1]S. Biesemans, [1]O. Richard, [1]H. Bender, [2]A. Azordegan, [2]J. McCormack, [3]S. Shirke, [3]J. Prochazka, [3]T. Long

[1] IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
[2]KLA-Tencor, 160 Rio Robles, San Jose, CA-95134, USA
[3]VLSI Standard, 3087 N 1st Street San Jose CA 95134, USA

As we move forward to the 45 and 32nm node, MuGFET's (Multi-Gate Field-Effect Transistor) are considered more and more as a necessary alternative to keep pace with Moore's Law. If proven manufacturable, MuGFET's could eventually replace conventional CMOS transistors within a few years. The ability to perform proper and extensive metrology in a production environment is then essential. We investigate here some of the requirements of MuGFET metrology. Accuracy and line width roughness (LWR) metrology will play an essential role, because the small dimension of the features involved. 3D metrology is required when dealing with non-planar devices. Sophisticated check of optical proximity correction (OPC) is needed in order to ensure that the design is respected. We propose here some possible solutions to address the needs of MuGFET metrology in a production-worthy fashion. A procedure to calibrate CDSEM to TEM for accuracy is developed. We performed LWR metrology of fins in a fully automated way by using CDSEM, while the 3D information is obtained by means of scatterometry. Finally, we will discuss the application of design-based metrology (DBM) to MuGFET OPC validation.

1. INTRODUCTION

The characterization of MuGFET's (Multi-Gate Field-Effect Transistor), or other two-dimensional (2D) devices, is a basic requirement in order to be able to adopt these architectures. A robust metrology approach is essential to characterize these structures. Accuracy, line width and sidewall roughness, three-dimensional (3D) characterization, patterning optimization are some of the issues that need to be solved in order to transfer this technology from development to production.

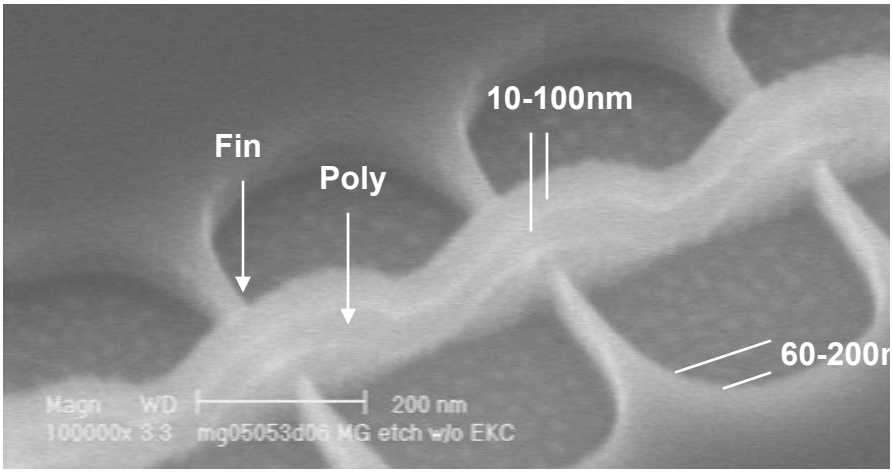

Figure 1: A MuGFET device.

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The fins of a MuGFET device, as shown in Fig. 1, can be as small as 10nm. This implies that beside the classical precision requirement, the metrology tools have to guarantee accuracy. A 5nm accuracy error would correspond to a 30% change in critical dimension (CD) when dealing with a 15nm feature, which is not acceptable. In the current development phase, the accuracy requirement is often satisfied by expensive characterization techniques, such as transmission electron microscopy (TEM) analysis. This approach is obviously not sustainable in a production environment.

Line width roughness (LWR) and sidewall roughness have a direct impact on device performance, and a robust metrology needs to be implemented in order to characterize these elements in both development and production. The requirement of 3D characterization of these devices is not common to any planar device metrology, and it is complicated by the small dimensions both in term of CD and height of MuGFET's. Finally, the accurate patterning of these small features requires a careful definition of the whole litho process.

In this paper we propose various solutions for some of the open issues related to MuGFET metrology. Accuracy standards in ranging from 10 to 70nm were developed to calibrate CDSEM tools. Scatterometry has been used to characterize the 3D structure of fins as small as 10nm. Design Based metrology (DBM) and on-line LWR characterization demonstrated to be able to optimize the litho process, and to quantify roughness in various process steps, respectively. Our results indicate the need to deliver a comprehensive metrology solution for MuGFET's, enabling to productize these advanced devices.

2. EXPERIMENTALS

All exposures are performed on an ASML PAS5500/1100 step-and-scan system, interfaced with a TEL Clean Track Act8. Maximum numerical aperture (NA) is 0.75. The total system is charcoal filtered to prevent airborne base contamination. Top-down CDSEM inspection is done on a KLA-Tencor eCD2. For the baseline technology integration work (front-end of line, FEOL), a 193nm resist from JSR, AR237J at 230nm Film Thickness (FT), is used on Brewer Science ARC29a organic Bottom Anti-Reflective Coating (BARC), FT = 77nm. The stack for MuGFET patterning (active layer) is 65nm silicon on 150nm buried oxide (= SOI stack, silicon-on-insulator). A 60nm TEOS oxide Hard-Mask (HM) is used during the patterning process for two reasons, providing etch resistance for the silicon etching and enabling CD (HM) trimming. A binary mask (BIM) is used to print an active pitch of 350nm; the CD at mask level is 120nm. The litho target is set at 100nm. This target is chosen to have acceptable process latitudes (CD control) in litho. Two exposure conditions are studied in more detail: a 0.63NA conventional 0.89σ and a 0.75NA annular 0.89 outer σ and 0.65 inner σ. The scatterometry measurements are done on a KLA Tencor Spectra FX100 using a polarized ellipsometer. The scatterometry target is 50x50 μm^2.

3. ACCURACY

Although the typical CDSEM resolution (2nm) does permit in principle metrology on small features such as gate length or fin width in MUGFET's (Multi-Gate FET), it is essential to develop the methodology to guarantee proper accuracy. Historically, the main deliverable of CD SEM tools has always been precision. This is understandable when dealing with features that are 50nm or larger. However, in case of a 15nm feature, even a 5nm error is not acceptable in a production environment.

In order to achieve this goal, accuracy standards in ranging from 10 to 70nm were developed. The calibrated CDSEM demonstrated to be sensitive to CD changes caused by process variations down to 10nm, and reference analysis performed on site previously measured by CDSEM confirmed the quality of the calibration.

We developed 4 different CD standards (70, 45, 25 and 13nm) by using the procedure described in Fig. 2 [1]. The standards were obtained by depositing alternating layers of silicon and silicon oxide (Fig. 2 left). The wafer is then diced and rotated, and the oxide is etched (Fig. 2 right). The uniformity of the CD is mainly dictated by the deposition uniformity, which can be carefully controlled. This permits to obtain standards having very low roughness. By using this procedure, it is possible to create features having an extremely uniform and well-controlled CD over various millimeters.

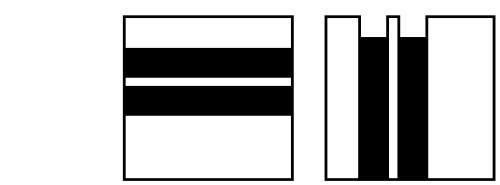

Figure 2: CD standard fabrication steps: (left) alternate layers of silicon (white) and silicon oxide (black) are deposited; (right) the wafer is then diced and rotated, and part of the oxide is etched, thus leaving a standing silicon line.

The sample is then certified NIST traceable by using TEM analysis. The CD of the line is measured by comparing it to the lattice constant of the crystalline silicon of the wafer, as shown in Fig. 3.

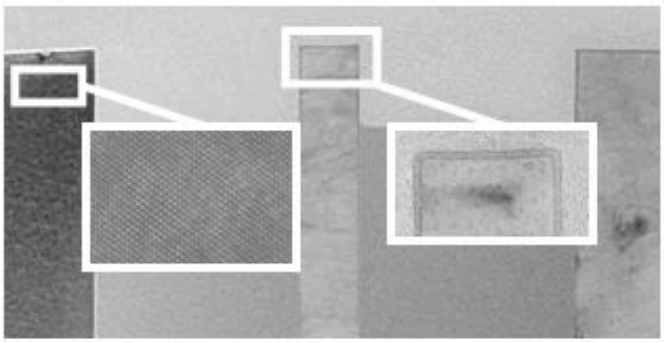

Figure 3: NIST traceability of the standards by comparison of the CD to the silicon lattice constants.

By using these accuracy standards, it was possible to optimize the measurement algorithm for accuracy. This step was obtained by mapping the total measurement uncertainty (TMU), as well as accuracy slope and intercept, as a function of the algorithm parameters. This procedure permitted to identify a single set of parameters that guarantee the best CDSEM accuracy in the range of interest. The measured precision after accuracy calibration was observed to be less than 1nm, and we believe it could still be improved.

In Fig. 4 we report the CD maps of fins on TEOS wafers after the corner rounding step. The fins are observed to be smaller in the middle of the wafer (~10nm) as compared to the edge of the wafer (~30nm). The radial pattern was confirmed on other wafers. These results indicate the sensitivity of the accuracy setting to process variation of features as small as 10nm.

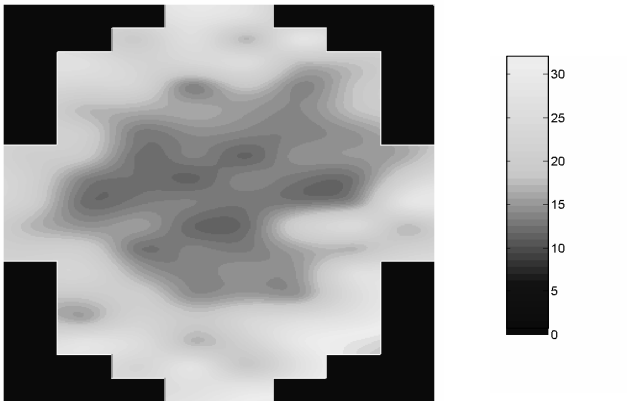

Figure 4: CD maps of a MUGFET wafer after corner rounding. Fins in the center of the wafer are smaller. The map shows the sensitivity of the calibrated CDSEM to process variations down to 10nm.

After performing a set of CDSEM measurements in well defined locations, the devices were measured with various reference techniques. In Fig. 5 (left) we compare the TEM on MUGFET devices before and after hydrogen annealing. The outer fins (first from the left) are clearly large of the inner fins, in agreement with the CDSEM results. Similarly, the TEM analysis confirmed that fins on the edge of the wafer are larger than those in the center of it, and that hydrogen annealing does reduce the fin's CD in the case of TEOS wafers. Finally, in Fig. 5 (right) we compare the compare the CD measured by the calibrated CDSEM to a variety of reference techniques, including TEM, XSEM, and scatterometry, as well as to the accuracy standards. The results clearly indicated the ability of the CDSEM to measure accurately in the range from 10 to 80nm.

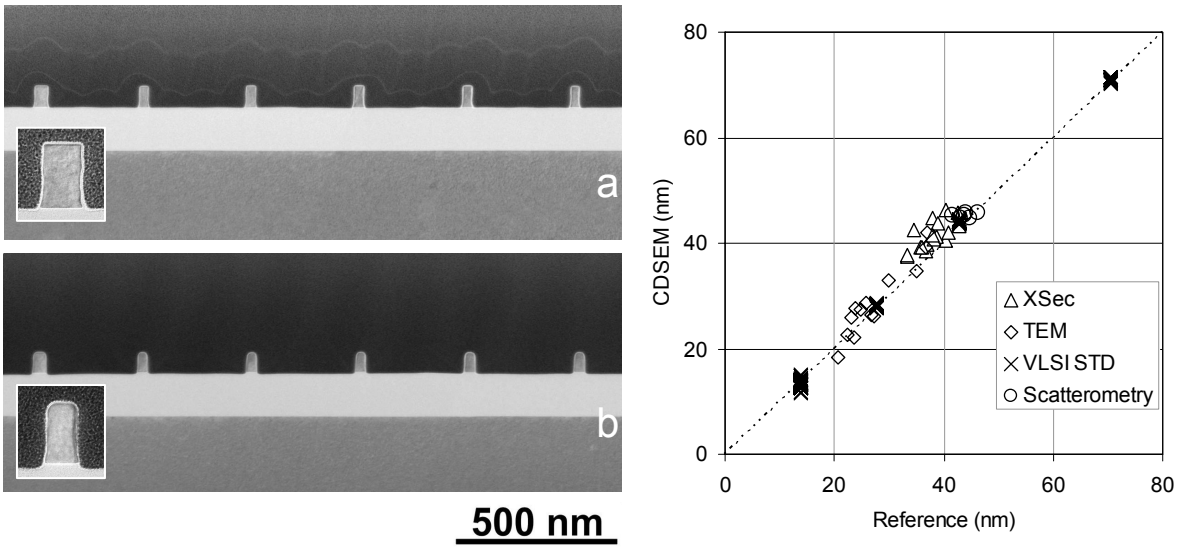

Figure 5: TEM of MUGFET devices (left) before (a) and after (b) hydrogen annealing on TEOS wafers. CDSEM measurements (right) versus reference measurements, indicating the ability of the calibrated CDSEM to measure accurately.

4. PATTERNING

In the case of MuGFET's, as for most structures, Critical Dimension (CD) variations through pitch and as function of length are not wanted, causing the devices to be non-reliable. In addition, the magnitude of corner rounding has direct impact on performances, increasing fin width and decreasing length, thus impacting short channel effects. Different methods can be used to reduce some of these effects, such as the addition of serifs or off-axis illumination settings.

A solid characterization of these approaches is needed, requiring a very large numbers of CDSEM measurements on different sites, which are extremely time consuming to set up. In order to overcome this issue, it is possible to use Design Based Metrology (DBM). This approach, originally introduced to improve design manufacturability, creates CDSEM recipes having hundreds of sites, starting from the design files. The recipes are created off-line in a few hours, whereas it would take days of tool time to create them manually.

In addition, it is critical to guarantee data integrity by adopting a methodology for reliable measurements based on proper 2D algorithms for the various metrology needs. In our analysis we used minimum/maximum gap and corner rounding algorithms. Gap algorithms are preferred for fin width and length measurements to standard line-width algorithms, which do not account for the rounding of the structures. The corner rounding algorithm determines the magnitude of the rounding (top-down) of the corners in a device. All algorithms are able to measure multiple structures within an image.

One of the main concerns with decreasing the size of the fins is the magnitude of corner rounding, which has an impact on both fin length and width. The rounding of the fin is characterized by the difference in area between the edge of the MuGFET and its bounding box. Corner rounding is reduced by off-axis illuminations as well as by serifs. We compare here annular and standard illumination, as well as three different OPC corrections, shown in Fig. 6.

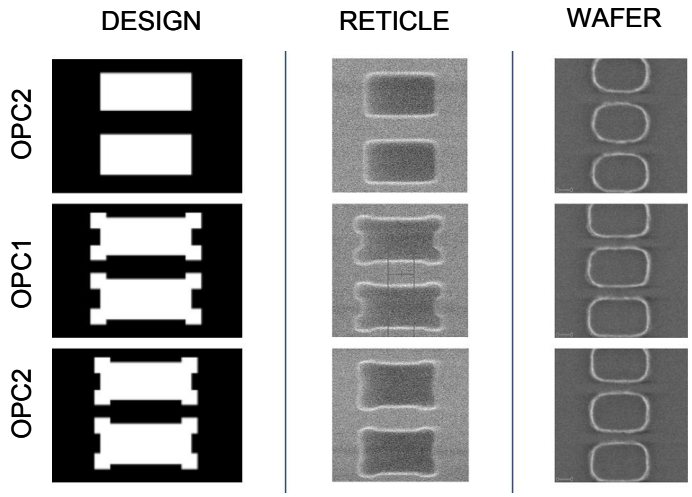

Figure 6: MuGFET device layout (with and without serifs) on design, reticle and after litho.

The quantitative results of the corner rounding analysis are shown in Fig. 7. The magnitude of the corner rounding is smaller for the shorter fins when an annular illumination is used. However, longer fins do not show an improvement in using annular illumination. Independently from the illumination type, the use of serifs does improve corner rounding for both long and short fins. We observe about an 8% improvement for regular illumination, as compared to an 18% improvement for annular. No difference is observed in between the two types of decoration.

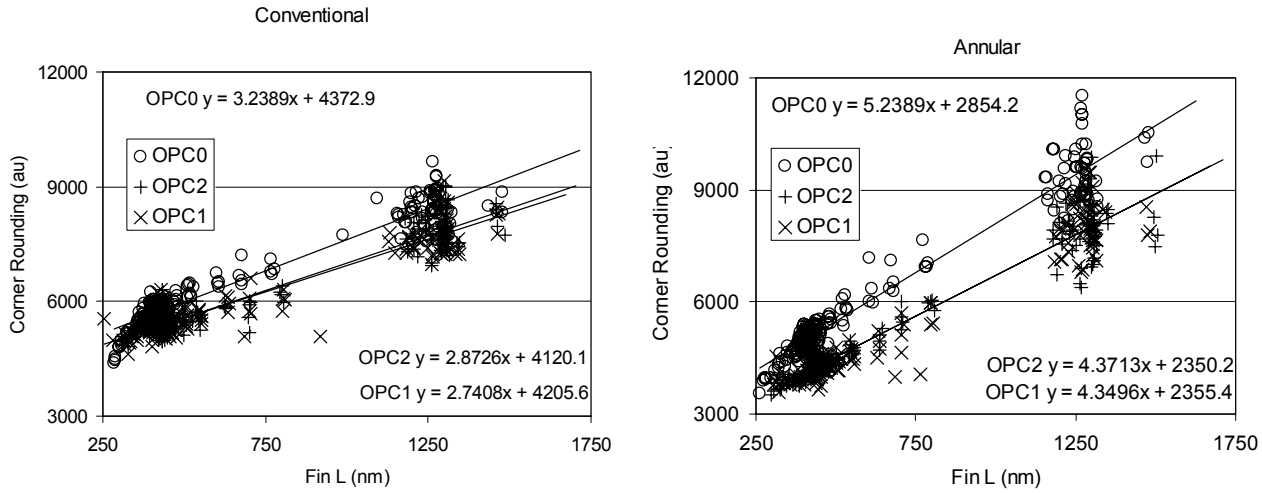

Figure 7: The magnitude of the rounded corner versus the fin length L for the different OPC versions for conventional and annular illumination.

Proximity effects for standard line and space patterns play a role in terms of CD uniformity within the multiple line structures, and outer fins are observed to be smaller as compared to inner fins after litho. In order to compensate for these artifacts, it is necessary to apply a proper bias that would guarantee CD uniformity. In Fig. 8 we report the ratio between inner and outer fin width of a multiple structure as a function of the biased outer fin. In this way, it is possible to define the best bias needed for the outer fin to print all fins on target. For the annular setting a bias of 20nm bias (outer fin of 140nm) is required. The effect for the non-symmetric and symmetric serifs is approximately same.

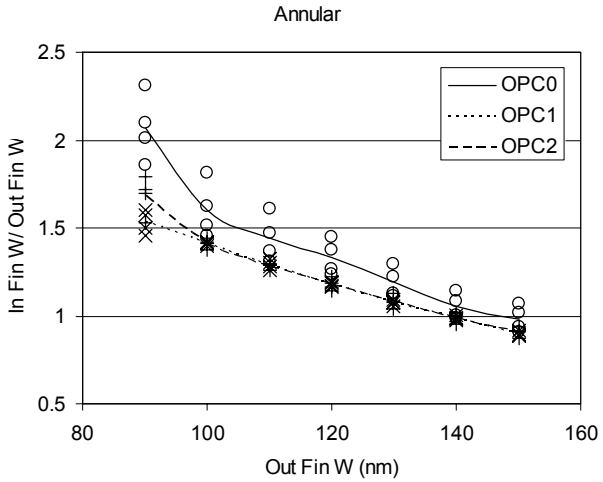

Figure 8: Ratio of inner and outer fin width versus the designed width of the outer fin.

Finally, we used DBM to support the creation of a resist model. In Fig. 9 we report the simulated 2D profiles and the corresponding CDSEM images. In addition, the simulations reproduced accurately the observed dependence of corner rounding on fin length. The fact that the model correlates well with the actual data permits its application to further optimization of the design.

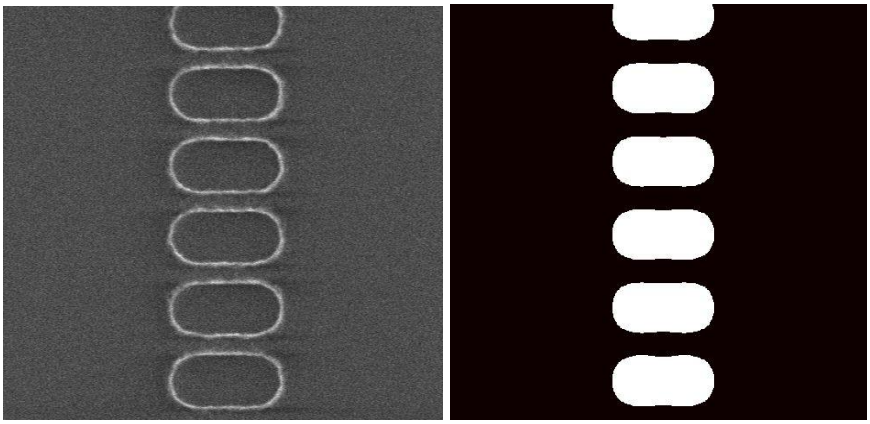

Figure 9: Example of the CDSEM image and the results of a lithographic simulation based on a resist model developed with DBM measurements.

5. LINE WITH ROUGHNESS

Another specific issue of MuGFET metrology is LWR. In term of top down line edge roughness, various frequencies will impact device performance differently [2]. Figure 10 reports an example of roughness on a fin. Low frequency LWR will impact mainly CDU, while high frequency components will impact device performance. It is then essential to fully characterize the spectral components and monitor LWR. Nowadays this can be done on-line by using the recently developed roughness algorithms available on CDSEM, able to report LWR, correlation length and power spectrum [3].

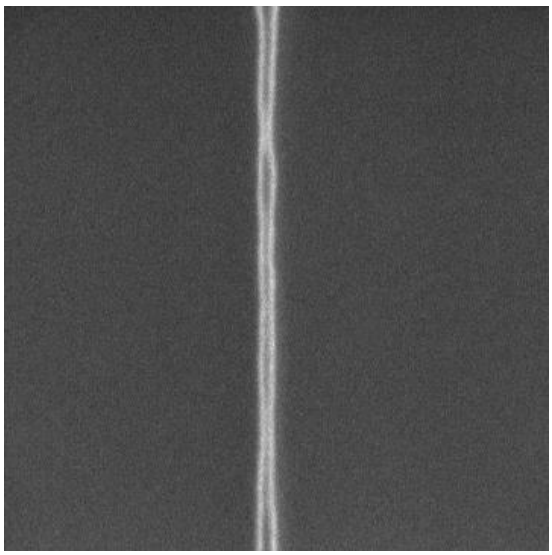

Figure 10: Line edge roughness on a fin (1 um FOV).

We tested the available CDSEM algorithms to demonstrate their sensitivity to MuGFET LWR. The results characterizing LWR for hydrogen annealing process step on SiON and TEOS substrate are reported in Fig. 11. The LWR distributions demonstrate clearly that the annealing does not improve the roughness characteristics for SION substrates (10%), while the improvement is significant on TEOS substrates (40%).

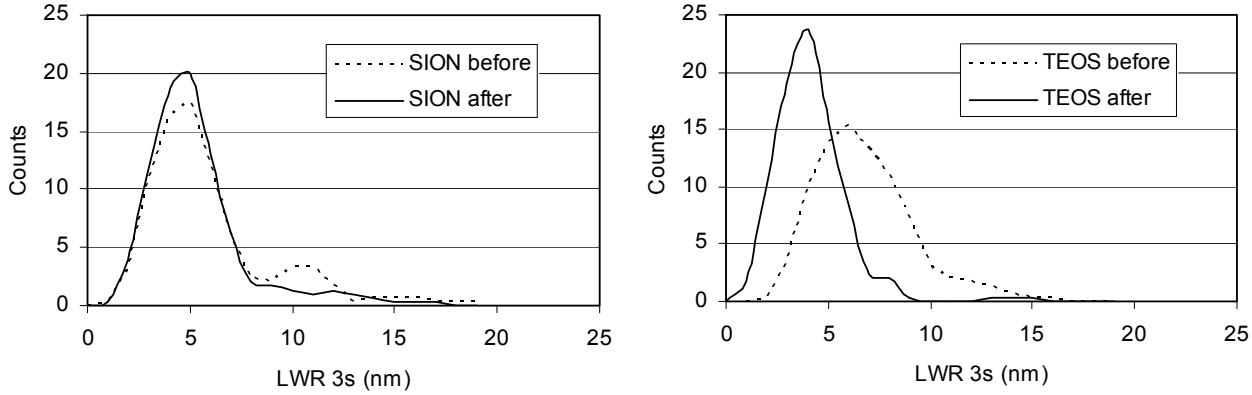

Figure 11: Comparison of the effect of hydrogen annealing on LWR in case of SiON (left) and TEOS (right) substrates

6. THREE-DIMENSIONAL CHARACTERIZATION

In order to implement a proper process control on MuGFET devices, it is crucial to be able to obtain 3D information on the device morphology. This requirement is quite complex when dealing with small features and large pitch, caused by resist trimming. We investigate here the capability of scatterometry to measure these devices.

The targets measured were not MUGFET devices but gratings with the same design rules on a flat surface of oxide. The CDSEM measurements of the two types of target used here were about 20nm and 40nm, respectively.

In Fig. 12 we report the scatterometry signals as a function of the wavelength, as measured on targets having line pitch ratio 100/100 and 150/150 after litho. For comparison, the spectrum of bare field oxide is shown, as measured next to the scatterometry targets. The CDSEM analysis of the 150/150 target shows dimension of 20-25nm fins with 300nm

pitch (1:15 ratio). The difference in the signals indicates that the system detects the presence of a design on the field oxide.

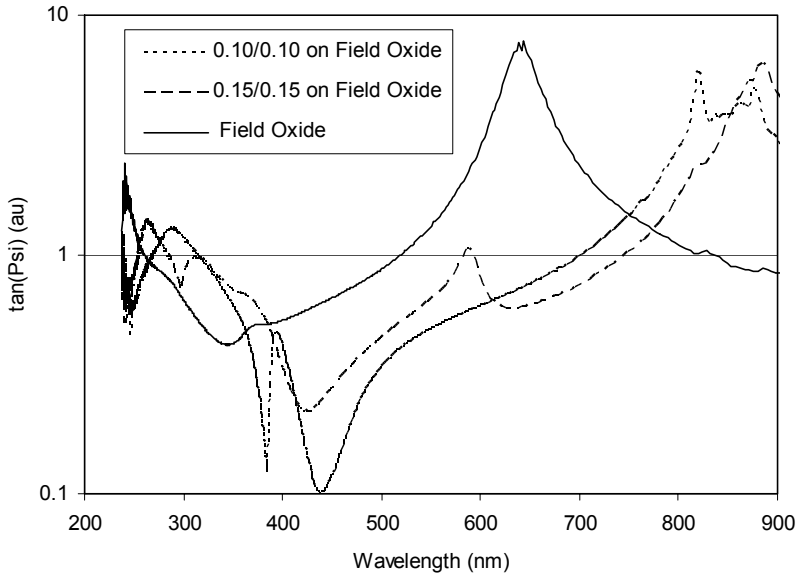

Figure 12: Scatterometry signals from fins (1:10, 1:15 line/pitch), compared to substrate.

A scatterometry model is built to fit the spectra obtained. The model uses 2 simple trapezoids, simulating the fin and the recess in oxide, respectively. The thickness and the profile of the recess are fixed parameters. In Fig. 13 we report the comparison of the reconstructed profile obtained by scatterometry, in good agreement with SEM cross section. The model shown here is not optimized but demonstrates the feasibility of such measurements. In addition, our preliminary test indicated good repeatability, suggesting the possibility that the current limit for scatterometry (1:8) could be extended. These results are encouraging, and indicate that scatterometry can indeed be the tool of choice for industrial monitoring of 3D for MuGFET's.

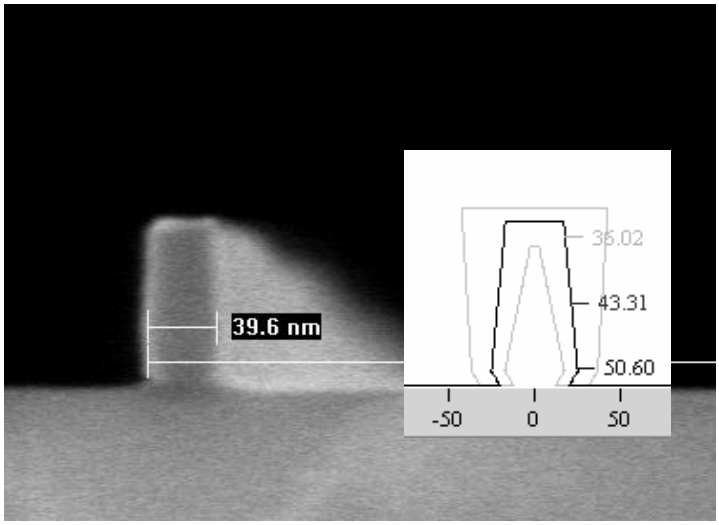

Figure 13: Modeled profile compared to X-section of the same target.

7. CONCLUSIONS

We propose several of approaches aimed to build a proper production metrology for MuGFET devices. In particular, we demonstrated a methodology to accurately calibrate a CDSEM, the need to use DBM in order to fine tune the patterning of the devices, the necessity of implementing on-line LWR analysis. Our preliminary results indicate the potential of scatterometry to extract 3D information. The results reported here indicate the feasibility of MuGFET metrology, although do not satisfy all the metrology requirements for these devices.

8. REFERENCES

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